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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,905	08/09/2001	Atsushi Kamashita	1113-016/MMM	6489

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EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/925,905

Applicant(s)

KAMASHITA ET AL.

Examiner

Paul E Brock II

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-24 and 40-55 is/are pending in the application.
- 4a) Of the above claim(s) 47-55 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 40-46 is/are allowed.
- 6) ☒ Claim(s) 18-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/177,254.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species I, claims 18 – 24 and 40 – 46 in Paper No. 6 is acknowledged. The traversal is on the ground(s) that claim 18 reads on all species and therefore should be considered a generic claim. Upon further consideration of applicant's argument, claim 18 is a generic claim that reads on all four species. Thus, claim 18 will be examined. However, claims 47 – 55 are species claims that read on the non-elected inventions. Therefore, claims 47 – 55 are continued to be withdrawn from consideration.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 18 – 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furumiya (USPAT 5637893, Furumiya) in view of the applicant's admitted prior art (AAPA).

With regard to claim 18, Furumiya discloses in figure 1b a method of transferring a charge from a charge accumulation layer to a transistor of a solid picture element so as to substantially eliminate residual images. Furumiya discloses in figure 1b locating a charge accumulation region (13) of a first conductive type (n) within a semiconductor substrate having a first surface such that no portion of the charge accumulation region contacts the first surface of

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the semiconductor substrate. Locating a depletion prevention region (17) within the semiconductor substrate between the charge accumulation region and the first surface. Locating a transfer gate (25) on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region. It is not clear if Furumiya discloses locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate for receiving a charge from the charge accumulation region and amplifying the charge. The AAPA teaches in figure 14 and page 2, lines 7 – 12 locating a transistor (205 – 209) within a semiconductor substrate (201), the transistor being in communication with a transfer gate (210) for receiving a charge from a charge accumulation region (203) and amplifying the charge. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the transistor of the AAPA in the method of Furumiya in order to amplify the photoelectrically converted charge as stated by the AAPA on page 2, lines 1 – 2.

With regard to claim 19, Furumiya discloses in figure 1b further comprising the step of locating the charge accumulation region so as to orient a first margin of the charge accumulation region toward a far edge of the gate and locating the depletion prevention region so that no portion of the depletion prevention region is closer to the far edge of the gate than the first margin of the charge accumulation region. It would have been further obvious in the method of Furumiya and the AAPA that this relationship with the far edge of the gate would also be true for the transistor.

With regard to claim 20, Furumiya discloses in figure 1b further comprising the step of locating a first margin of the charge accumulation region 0.0 microns closer to the far edge of the gate than any portion of the depletion prevention region. It would have been further obvious in

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the method of Furumiya and the AAPA that this relationship with the far edge of the gate would also be true for the transistor.

With regard to claim 21, the AAPA teaches on page 2, line 1 wherein the transistor is a field effect transistor.

With regard to claim 24, Furumiya discloses in figures 1b wherein the transfer gate is a metal-oxide semiconductor gate.

4. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furumiya and the AAPA as applied to claim 18 above, and further in view of Gross (USPAT 5734293).

The AAPA teach that the transistor is a JFET type. Furumiya and the AAPA do not teach wherein the transistor is a bipolar transistor or a metal-oxide semiconductor transistor. Gross teaches in column 8, lines 39 – 46 wherein an amplifying transistor is a JFET type or a bipolar transistor or a metal-oxide semiconductor transistor. It would have been obvious to one of ordinary skill in the art to use the bipolar of metal-oxide semiconductor transistor of Gross as a substitute for the JFET of Furumiya and the AAPA in order to maintain the condition that an input bias of a voltage feedback smaller than an input bias of a current feedback amplifier as stated by Gross in column 8, lines 39 – 46. This gives one of ordinary skill in the art the ability to choose transistors based on the technology employed on other areas of the integrated device while not adding additional process steps.

Allowable Subject Matter

5. Claims 40 – 46 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
August 15, 2003

